REMARKS

By this response, claims 1-17 are pending, of which claim 1 is amended. The claim is amended to correct clerical errors but the claim scope is not narrowed thereby for any reason relating to patentability. No new matter has been added.

The Office Action dated January 25, 2002 allowed claims 11-13, rejected claims 4, 11, and 14 under 35 U.S.C. §103(a) as being unpatentable over Ooishi (U.S. Patent No. 6,324,118), and objected to claims 2, 3, 5-10, and 15-17 as being depending from a rejected base claim, but would be allowable if rewritten in independent form. The rejection and objection are respectfully traversed in light of the remarks presented herein.

REJECTION OF CLAIMS UNDER 35 U.S.C. §103

Claims 1, 4 and 14 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Ooishi (U.S. Patent No. 6,324,118). Ooishi, however, does not support a prima facie case of obviousness because Ooishi is not an effective reference under 35 U.S.C. 103.

According to 35 U.S.C. §103(c), if a reference qualifies as prior art only under 35 U.S.C. 102(e), the reference cannot preclude patentability under §103 where the application and the reference were commonly owned when the invention was made. Both Ooishi and the current application are assigned to and commonly owned by Mitsubishi Denki. Moreover, Ooishi qualifies as prior art only under 35 U.S.C. 102(e), as the current application has an earlier application date than the issue date of Ooishi. Thus, Ooishi is not an effective reference under 35 U.S.C. §103 and cannot support a prima facie case of obviousness. Therefore, the obviousness rejection based on Ooishi is untenable and should be withdrawn.

Claims 2, 3, 5-10 and 15-17 were objected to as being depending from claim 1. As discussed above, the obviousness rejection of claim 1 is untenable and should be

withdrawn. Therefore, the objection to claims 2, 3, 5-10 and 15-17 should also be withdrawn. Favorable consideration of the claims is respectfully requested.

CONCLUSION

Therefore, the present application claims subject matter patentable over the references of record and is in condition for allowance. Favorable consideration is respectfully requested.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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VERSION WITH MARKINGS SHOWING CHANGES MADE

IN THE SPECIFICATION

Please replace the paragraph starting from page 24, line 2, with the following paragraph:

--Reference will now be made to Fig. 16 to describe an exemplary configuration of a semiconductor device 20000 having DLL 2000 of the second embodiment. Semiconductor device 20000, as shown in Fig. 16, includes DLL 2000 receiving external clocks CLKext and ZCLKext, an input buffer 2001 receiving a control signal (a row address strobe signal /RAS, a column address strobe signal/CAS, a chip select signal /CS, a write enable signal /WE and the like), an input buffer 2002 receiving an address signal An, wherein n = 0, 1, ... 11, and bank address signals BA0 and BA1, a control signal generation circuit 2003 receiving an output of input buffer 2001 to generate an internal control signal, a row address latch 2004 responsive to the internal control signal for latching a row address output from input buffer [1002] 2002, a column address latch 2005 responsive to the internal control signal for latching a column address output from input buffer 2002, a memory array 2006 having a plurality of memory cells arranged in rows and columns, and a plurality of word lines arranged in the direction of the rows and a plurality of bit lines arranged in the direction of the columns, a row decoder 2007 responsive to the internal control signal for selecting a row corresponding to an output of row address latch 2004, and a column decoder 2008 responsive to the internal control signal for selecting a column corresponding to an output of column address latch 2005. Input buffers 2001 and 2002 take a received signal in in synchronization with clock BUFFCLK (or CLKin3) output from DLL 2000. Clock CLKin3 is more suitable for rapid operation than clock BUFFCLK.--

IN THE CLAIMS

1. (Amended) A delay locked loop comprising:

a delay circuit delaying a first clock to output a second clock;

a detector detecting a phase difference between said first and second clocks; and

a gray code counter using a gray [cord] code, responsive to an output of said detector for generating a signal adjusting an amount of delay of said delay circuit.